**Printout 1/2**

NET "Clk" LOC = P6 ;

NET "up\_down" LOC = P7 ;

NET "enable" LOC = P8 ;

NET "clr" LOC = P9 ;

NET "d<3>" LOC = P1;

NET "d<2>" LOC = P2;

NET "d<1>" LOC = P3;

NET "d<0>" LOC = P4;

NET "q<3>" LOC = P35;

NET "q<2>" LOC = P36;

NET "q<1>" LOC = P37;

NET "q<0>" LOC = P38;

`timescale 1ns / 1ps

module lllll(clk , up\_down , enable , clr , q ,d );

input clk , up\_down , enable , clr;

output[3:0]q;

input[3:0]d;

reg[3:0]tem = 4'b0000;

always@(clk,clr)begin

if(clr)

tem = 4'b000;

else

if(!enable)

tem = d;

else

if(up\_down)

tem = tem + 1'b1;

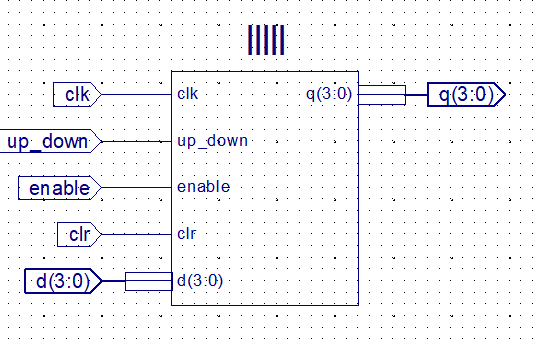
else

tem = tem - 1'b1;

end

assign q = tem;

endmodule



**printout 2/2**

NET "clk" LOC = P1;

NET "q\_2hz" LOC = P11;

NET "q\_083hz" LOC = P12;

`timescale 1ns / 1ps

module sdsd(input clk,output q\_2hz,q\_083hz);

reg rq\_2hz = 1'b0;

reg rq\_083hz = 1'b0;

reg[23:0]Counter\_2hz = 0;

reg[23:0]Counter\_083hz= 0;

parameter fin = 20\_000\_000;

parameter fout\_2hz = 2;

parameter Coust\_2hz = fin/(2\*fout\_2hz);

parameter fout\_083hz = 083;

parameter Coust\_083hz = fin/(2\*fout\_083hz);

always@(posedge clk)

begin

Counter\_2hz <= Counter\_2hz+1'b1;

Counter\_083hz <= Counter\_083hz+1'b1;

if(Counter\_2hz == Coust\_2hz)

begin

Counter\_2hz <= 0;

rq\_2hz <= ~rq\_2hz;

end

if(Counter\_083hz == Coust\_083hz)

begin

Counter\_083hz <= 0;

rq\_083hz <= ~rq\_083hz;

end

end

endmodule